

Court Skinner  
310 Donohoe Street  
East Palo Alto, CA 94303  
[court@courtskinner.com](mailto:court@courtskinner.com)

Phone: 650 353 1646

**Education:** Ph.D., Physics of Solids, Massachusetts Institute of Technology 1966

## **Experience:**

### **Consultant**

Main client: Semiconductor Research Corporation 1998 to 2001

Charged with recruiting new members to the SRC and managing the SRC West Coast Office. Primarily involved in setting up meetings between the research organizations of prospective members and the SRC senior management. Also working on a marketing view of the SRC as Pioneer in Collaborative Research. In addition am participating as co-chair of the Factory Integration Chapter of the ITRS (International Technology Roadmap for Semiconductors), chairing the SEMI North American Awards Committee, and acting as secretary for the ISSM (International Symposium for Semiconductor Manufacturing) executive committee.

### **National Semiconductor Corporation**

Director, System Technology Integration 1997 to 1998

Charged with integrating the design requirements of design rules, circuit models, cell libraries and design flows and tools into a single comprehensive product to support a deep submicron CMOS technology configuration. Team building, internal customer education, project management, change management were significant requirements for success.

Director, Research Center 1988 to 1997

Directing research programs in semiconductor manufacturing science including computer integrated manufacturing (CIM), submicron scale integrated circuit process development, materials analysis, unit processes for thin film deposition, lithography and etching, establish cross organizational teams to execute internal and government funded research projects/programs.

Research Project Manager and SRC Liaison 1983 to 1988

Executive technical advisory board member representing National Semi, Established manufacturing science as separate discipline for SRC funding, helped set up the Manufacturing Competitiveness Panel, SEMATECH, and the International Symposium on Semiconductor Manufacturing, elected member of IEEE Electron Device Society Administrative Committee, Active in the SEMI standards activities.

Manager, Advanced Wafer Fab Engineering 1978 to 1983

Hired to establish National Semi's first process technology research department. Won contract for government funded VHSIC (Very High Speed Integrated Circuits) program as partner with Westinghouse Electric and learned hard lessons in management and the establishment of expectations.

### **Advanced Micro Devices**

EPROM Process Development Engineer 1976 to 1978

Product/process engineer taking 8K EPROM from design phase to successful prototype production. Learned valuable communication skills and problem solving approaches for working in large, difficult to control groups with minimum resources.

### **Data General Corporation**

Director, MOS Process Development 1972 to 1976

Built fabrication facility from the ground up learning all the technologies from building construction, ultra clean water plant operation, to wafer process design and operations management

### **American Micro Systems**

Process Development Engineering Manager 1970 to 1972

Learned basics of MOS integrated circuit process technology and, more importantly how to get experiments done in a complex production oriented environment by establishing good working relationships with those more experienced than I in the nuts and bolts of the operations. Designed research Fab, which was scrapped when production operations' yield increased and left them with one too many fab facilities.

### **Motorola**

Process Engineer 1966 to 1970

Set up thin film deposition equipment and developed computer models to characterize the process technology.